	Type	Hits	Search Text	DBs	Time Stamp
1	IS&R	1553	(257/326,347).CCLS.	USPAT; US-PGPUB	2003/05/30 09:48
2	BRS	283	((257/326,347).CCLS.) and @pd>20021023	USPAT; US-PGPUB	2003/05/30 09:49
3	IS&R	146	(257/326).CCLS.	USPAT	2003/05/30 10:48
4	IS&R	0	(257/185.13).CCLS.	USPAT	2003/05/30 10:49
5	IS&R	248	(365/185.13).CCLS.	USPAT	2003/05/30 10:51
6	IS&R	286	(365/185.05).CCLS.	USPAT	2003/05/30 10:51
7	BRS	4	("4442510" | "5471422" | "5576989" | "5592001").PN.	USPAT	2003/05/30 12:46
8	BRS	7	("5515318" | "5604699" | "5712816" | "5761125" | "5774395" | "5793675" | "5909397").PN.	USPAT	2003/05/30 12:48
9	BRS	3	("5883826" | "6147911" | "6037785").PN.	USPAT	2003/05/30 12:49
10	BRS	8	("4302766" | "4420871" | "4816883" | "4907197" | "5021848" | "5049516" | "5081054" | "5216268").PN.	USPAT	2003/05/30 13:21
11	BRS	24	5471422.URPN.	USPAT	2003/05/30 13:22

	D cument ID △	Pages	Title	Current OR	Current XRef	Inventor
1	US 5471422 A	10	EEPROM cell with isolation transistor and methods for making and operating the same	365/185.26	257/314; 257/315; 257/E27.103; 257/E29.304; 365/182; 365/218	Chang, Ko-Min et al.
2	US 6014328 A	52	Memory cell allowing write and erase with low voltage power supply and nonvolatile semiconductor memory device provided with the same	365/185.05	257/E21.68; 257/E27.103; 365/185.17	Onakado, Takahiro et al.
3	US 6128219 A	23	Nonvolatile memory test structure and nonvolatile memory reliability test method	365/185.09	365/185.05; 365/185.24; 365/201	Pio, Federico et al.
4	US 6426895 B2	32	Memory system and programming method thereof	365/185.19	365/185.05; 365/185.12; 365/185.23	Kosaka, Hideo et al.